UNIT 4
INTEGRATED CIRCUIT DESIGN METHODOLOGY
E5163
LEARNING OUTCOMES

4.1 DESIGN METHODOLOGY

By the end of this unit, student should be able to:

1. Explain the design methodology for integrated circuit.
2. Draw the tree diagram of design methodologies for integrated circuit.
3. Define ASICs methodology for integrated circuit.
4. Discuss the advantages of specific-custom IC (ASICs) over standard IC.
DEFINITION

• **Integrated Circuit Design**, or **IC design**, is a subset of **electrical engineering** and **computer engineering**, encompassing the particular **logic and circuit design techniques** required to design **integrated circuits**.

• **Integrated Circuits** consist of miniaturized **electronic components** built into an **electrical network** on a monolithic **semiconductor substrate** by **photolithography**.
DIGITAL IC DESIGN

• IC design can be divided into the broad categories of digital and analog IC design.

• Digital IC design is to produce components such as microprocessors, FPGAs, memories (RAM, ROM, and flash) and digital ASICs.

• Digital IC design focuses on logical correctness, maximizing circuit density, and placing circuits so that clock and timing signals are routed efficiently.
ANALOG IC DESIGN

• Analog IC design also has specializations in power IC design and RF IC design. Analog IC design is used in the design of op-amps, linear regulators, phase locked loops, oscillators and active filters. Analog IC design is more concerned with the physics of the semiconductor devices such as gain, matching, power dissipation, and resistance. Fidelity of analog signal amplification and filtering is usually critical and as a result, analog ICs use larger area active devices than digital designs and are usually less dense in circuitry.
TREE DIAGRAM OF INTEGRATED CIRCUIT DESIGN METHODOLOGY
ASICs

• Definition: An integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC.

• Why using ASIC?
  • Higher reliability
  • Faster turn-around time (total time taken between the submission of a program for execution and the return of the complete output to the customer.)
  • Tighter security
  • Lower non-recurring cost (unusual charge, expense or lost that is unlikely to occur again in the normal course. Ex: design, development or loses. Also called extraordinary cost)
  • Better performance
## ADVANTAGES OF ASIC

**Advantages**
- Efficient use of board space (lower final system cost)
- Product security
- Unique features and fine-tuning the product
- Optimized system performance

**Disadvantages**
- Potential for design failure
- Not off-the-shelf available (specification, design, testing and documentation phases are needed)
- High unit cost of IC (higher initial costs of development)

Fine-tuning refers to circumstances when the parameters of a model must be adjusted very precisely in order to agree with observation.
## Specific—costum IC VS Standard IC

<table>
<thead>
<tr>
<th>Standard IC</th>
<th>ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typically low component cost</td>
<td>Good security of intellectual property</td>
</tr>
<tr>
<td>Parts available off the shelf</td>
<td>Optimum system design</td>
</tr>
<tr>
<td>Low or insignificant IC design cost</td>
<td>Relatively efficient use of board space (smaller systems)</td>
</tr>
<tr>
<td>Proven component reliability</td>
<td>Reliability enhanced at system level (fewer components)</td>
</tr>
<tr>
<td>Multiple sourcing</td>
<td>Performance may be better than comparable standard ICs (unique</td>
</tr>
<tr>
<td>System house not required to have in-house experts in chip design</td>
<td>features and lower power consumption)</td>
</tr>
</tbody>
</table>

Multiple sourcing is the practice of buying in items from more than one source to reduce the risk of production or sales being disrupted from any problems that may take place in the supply chain.
LEARNING OUTCOMES

4.2 FULL-CUSTOM DESIGN

By the end of this unit, student should be able to:

1. Explain the full-custom methodology for integrated circuit.
2. Explain the semi-custom methodology for integrated circuit.
3. Discuss the advantages and disadvantages of full-custom methodology.
4. Discuss the advantages and disadvantages of semi-custom methodology.
DEFINITION

• Full-custom IC design is a methodology for designing integrated circuits by specifying the layout of each individual transistor and the interconnections between them.

• Full-custom IC design potentially maximizes the performance of the chip, and minimizes its area, but is extremely labor-intensive to implement.

• Full-custom IC design is limited to ICs that are to be fabricated in extremely high volumes, notably certain microprocessors and a small number of ASICs. Time taken to design IC is longer and slow.

• A full-custom IC includes some (possibly all) logic cells that are customized and all mask layers that are customized.

• Therefore, full-custom ICs are the most expensive to manufacture and to design.

• Example: microprocessor.
DEFINITION

• Semi-custom IC design is a methodology for making an integrated circuit which a portion of the circuit function is **predefined and unalterable**, while other portions can be **configured** to meet the designer's specific needs.

• Designers have the capability of designing application-specific circuits themselves, **using either standard cell libraries or preconfigured arrays**.

• In semicustom IC, all of the logic cells are predesigned and some (possibly all) of the mask layers are customized. Using predesigned cells from a cell library makes our lives as designers much easier and faster.

• Therefore, semi-custom ICs are the **less expensive to manufacture and to design**.

• Examples: ethernet chip, hard disk controller
FULL-CUSTOM IC DESIGN

<table>
<thead>
<tr>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. substantial reduction in die (chip) area.</td>
<td>1. Increase design time.</td>
</tr>
<tr>
<td>2. Ability to integrate analog component and pre-designed components.</td>
<td>2. Large amount of design expense and effort.</td>
</tr>
<tr>
<td>3. High degree of optimization in performance and area.</td>
<td>3. Complexity and highest risk.</td>
</tr>
</tbody>
</table>

SEMI-CUSTOM IC DESIGN

<table>
<thead>
<tr>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. rapid turn around.</td>
<td></td>
</tr>
<tr>
<td>2. design is performed at the logic gate level.</td>
<td></td>
</tr>
<tr>
<td>3. simplified verification.</td>
<td></td>
</tr>
</tbody>
</table>
4.3 SEMI-CUSTOM DESIGN

By the end of this unit, student should be able to:

1. Explain the gate-array methodology.
2. State and draw the basic elements in CMOS gate-array.
3. Discuss the advantages and disadvantages of gate-array methodology.
4. Discuss two (2) methods to increase the percentage of gate used.
DEFINITION

- A gate array or uncommitted logic array (ULA) is an approach to the design and manufacture of application-specific integrated circuits (ASICs).
- A gate array circuit is a prefabricated silicon chip circuit with no particular function in which transistors, standard NAND or NOR logic gates, and other active devices are placed at regular predefined positions and manufactured on a wafer.
- Parts of the chip (transistors) are pre-fabricated, and other parts (wires) are custom fabricated for a particular customer’s circuit. Accomplished by adding layers of metal interconnects to the chips.
- Two types of gate array:
  - Traditional (channeled) Gate Array
  - Sea-of-Gate Gate Array - the routing is performed over the gates, hence more metal layers required, but the gate density is much higher than in a channel gate array.
## GATE ARRAY

<table>
<thead>
<tr>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Low Cost</strong> Gate Arrays can be purchased for less than a dollar per unit. And for a given process, they can be packaged smaller than FPGAs, thereby reducing the circuit area and contributing to a reduction of total cost.</td>
<td><strong>1. performance not as good as full-custom or standard-cell-based ICs.</strong></td>
</tr>
<tr>
<td><strong>2. Stabilization of component procurement (perolehan)</strong> Gate Array is a custom product, and can hence be delivered in stable quantities based on your demand forecast information.</td>
<td><strong>2. Non optimizing spacing and excess circuitry.</strong></td>
</tr>
<tr>
<td><strong>3. Security</strong> With Gate Arrays, the customer’s proprietary circuit design is hard-wired onto the semi-custom ICs, making it impossible to duplicate. When using FPGA, the customer's proprietary circuit data is stored on a ROM, and FPGA is a general-purpose product. Hence, the circuit data can be intercepted and duplicated by monitoring the bit stream between the ROM and the FPGA during start-up.</td>
<td><strong>3. Limited transistor sizing options in terms of density, performance and power.</strong></td>
</tr>
<tr>
<td><strong>4. shorter manufacture lead time</strong></td>
<td><strong>4. Wiring blockage and inefficiencies</strong></td>
</tr>
</tbody>
</table>


GATE ARRAY

• Two (2) methods to increase the percentage of gate used:
  – Using the same design.
LEARNING OUTCOMES

4.3 SEMI-CUSTOM DESIGN

By the end of this unit, student should be able to:

1. Explain the standard cells methodology.
2. Draw a design layout of standard cells.
3. Discuss the advantages and disadvantages of standard cells methodology.
DEFINITION

• **Standard Cell** methodology is a method of designing application-specific integrated circuits (ASICs) with mostly digital-logic features. Standard cell methodology is an example of design abstraction, whereby a low-level very-large-scale integration (VLSI) layout is encapsulated into an abstract logic representation (such as a NAND gate).

• Standard Cell is a group of transistor and interconnect structures that provides a Boolean Logic function (e.g., AND, OR, XOR, XNOR, inverters) or a storage function (flipflop or latch). The simplest cells are direct representations of the elemental NAND, NOR, and XOR boolean function.

• Two types:
  • Channelled Cells
  • Channel-less Cells
Characteristic of the Cells

- Each cell is designed with a fixed height.
  - To enable automated placement of the cells, and
  - Routing of inter-cell connections.
  - A number of cells can be abutted side-by-side to form rows.
- The power and ground rails typically run parallel to upper and lower boundaries of cell.
  - Neighboring cells share a common power and ground bus.
  - nMOS transistors are located closer to the ground rail while the pMOS transistors are placed closer to the power rail.
- The input and output pins are located on the upper and lower boundaries of the cell.
Standard Cells

- Made to stack side-by-side
  - Fixed height
  - Width can vary
  - Can abut at Vdd & GND (without any design rule errors)
Standard Cell Layout
Standard cells
Standard Cell Layout

Note uniform height

Routing Channel

Feed-through cell

Routing Channel
# STANDARD CELLS

<table>
<thead>
<tr>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. More flexible to include digital as well as analog functions.</td>
<td>1. Costs in additional mask-making, software, and workstation resources</td>
</tr>
<tr>
<td>2. More compact design (less routing area, improved speed)</td>
<td>2. Wasted chip area will be high due to the area occupied by the wiring channels can exceed 50% of the internal chip. This problem can be greatly reduced by using multiple metal layers in chip designs.</td>
</tr>
<tr>
<td>3. More sophisticated systems can be built (using parameterized cells, microprocessors)</td>
<td>3. No saving in fabrication time due to no prefabricated cells.</td>
</tr>
<tr>
<td><em>Parameterized</em>: n-bit counters, shift registers, PLAs, RAMs, ROMs.</td>
<td></td>
</tr>
</tbody>
</table>


LEARNING OUTCOMES

4.3 SELECTION CRITERIA

By the end of this unit, student should be able to:

1. State the design methodology selection criteria.
2. Compare the design methodologies based on the criteria in 1.
Design Methodology Selection

Criteria

• The choice of design style depends on the intended functionality of the chip, time to market and total number of chips to be manufactured.

• Full custom design is used for microprocessors and other complex volume applications.

• While FPGA may be used for simple and low volume applications.

• For large circuits, it is common to partition the circuit into smaller subcircuits which are designed using different team.

• Each team may use different design.
Choice of Design Methodologies

- Design freedom/effort
- Interconnection density
- Performance
- Security
- Production volume
- Turn-around time
- Reliability

??
## Comparison of Design Styles

<table>
<thead>
<tr>
<th></th>
<th>Full-Custom</th>
<th>Standard Cell</th>
<th>Gate Array</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell size</td>
<td>variable</td>
<td>fixed height</td>
<td>fixed</td>
<td>fixed</td>
</tr>
<tr>
<td>Cell type</td>
<td>variable</td>
<td>variable</td>
<td>fixed</td>
<td>programmable</td>
</tr>
<tr>
<td>Cell placement</td>
<td>variable</td>
<td>in row</td>
<td>fixed</td>
<td>fixed</td>
</tr>
<tr>
<td>Interconnections</td>
<td>variable</td>
<td>variable</td>
<td>variable</td>
<td>programmable</td>
</tr>
<tr>
<td>Fabrication layers</td>
<td>all layers</td>
<td>all layers</td>
<td>routing layers only</td>
<td>no layers</td>
</tr>
</tbody>
</table>


## Comparison of Design Styles

<table>
<thead>
<tr>
<th></th>
<th>Full-Custom</th>
<th>Standard Cell</th>
<th>Gate Array</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area</strong></td>
<td>compact</td>
<td>compact to moderate</td>
<td>moderate</td>
<td>large</td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>high</td>
<td>high to moderate</td>
<td>moderate</td>
<td>low</td>
</tr>
<tr>
<td><strong>Design cost</strong></td>
<td>high</td>
<td>medium</td>
<td>medium</td>
<td>low</td>
</tr>
<tr>
<td><strong>Time-to-market</strong></td>
<td>long</td>
<td>medium</td>
<td>medium</td>
<td>short</td>
</tr>
</tbody>
</table>
Comparing Technologies - Density (gates per chip)

- Highest to lowest density:
  - Full Custom,
  - Standard Cell,
  - Gate Array,
  - FPGAs,
  - CPLD,
  - PLD

- Full Custom, Standard Cell, Gate Array are called ASIC technologies (Application Specific Integrated Circuit).

- Large Density gap between ASIC technologies and Programmable logic technologies (FPGAs, CPLD, PLD).

- Highest end FPGA density is now equal to low-end ASIC density (i.e., hundreds of thousands of gates with embedded SRAMs).
Comparing Technologies - Speed

- Highest to lowest performance: Full Custom, Standard Cell, Gate Array, PLDs, CPLDs, FPGAs.
- Again, large performance gap between ASIC technologies and programmable technologies.
- Performance of programmable technologies is in reverse order of their densities.
Comparing Technologies - Cost

- Depends heavily on volume.
- If only need a few hundred, then FPGAs can be cheaper.
- If need thousands, then ASIC technologies are cheaper.
- NRE cost (non-recurring engineering costs) are higher for ASIC technologies than FPGAs
- Per-unit-cost (chip cost) higher for FPGAs
Summary

- Full custom can give best density and performance.
- Faster design time and ease of design are principle advantages of gate array and standard cell over full custom.
- Fast fabrication time and lower cost are principle advantages of gate arrays over standard cell.
- Gate arrays offer much higher density over FPGAs and are cheaper than FPGAs in volume production.
Summary (cont.)

- FPGAs' principle advantage over gate arrays is 'instant' fabrication time (programmed on desktop). FPGAs are also cheaper than gate arrays in low volume.
- Densities are reaching 100's of thousands of gates/chip.
- Can be used to prototype full custom/standard cell designs.
- PLDs still hold a speed advantage over most FPGAs are useful primarily for high speed decoding and speed critical glue logic.
Sources

- Bob Reese
- Rob Yates
- Sheffield Hallam University
- Mark L. Chang <mchang@ece.nwu.edu>